

Docket No.: 0152-0703PUS1  
(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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In re Patent Application of:  
Hisashi YAMADA et al.

Application No.: 10/524,013

Confirmation No.: 7576

Filed: February 8, 2005

Art Unit: 2823

For: METHOD FOR PRODUCING COMPOUND  
SEMICONDUCTOR WAFER AND  
COMPOUND SEMICONDUCTOR DEVICE

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Examiner: M. Estrada

**REPLY TO RESTRICTION REQUIREMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In reply to the Restriction Requirement dated February 6, 2006, the following remarks are respectfully submitted in connection with the above-identified application.

This reply includes: remarks.

**REMARKS**

Claims 1-6 are pending in the present application.

The Examiner has required election in the present application between:

Group I, claims 1-4; and

Group II, claims 5-6.

**For the purpose of examination of the present application, Applicants elect, without traverse, Group I, Claims 1-4.**

**CONCLUSION**

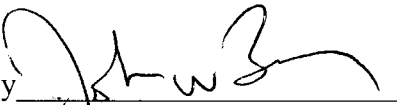
Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John W. Bailey, Registration No 32,881 at the telephone number below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

- ☐ Attached is a Petition for Extension of Time.
- ☐ Attached hereto is the fee transmittal listing the required fees.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to our Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under § 1.17; particularly, extension of time fees.

Dated: February 28, 2006

Respectfully submitted,

By 

John W. Bailey

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